HIGH DENSITY SEMICONDUCTOR MEMORY CELL AND MEMORY ARRAY USING A SINGLE TRANSISTOR HAVING A BURIED N+ CONNECTION

RELATED APPLICATIONS

[0001] This application is a continuation-in-part of co-pending U.S. Patent Application Serial No. 10/448,505 filed May 30, 2003 entitled "HIGH DENSITY SEMICONDUCTOR MEMORY CELL AND MEMORY ARRAY USING A SINGLE TRANSISTOR" and co-pending U.S. Patent Application Serial No. 10/133,704 filed April 26, 2002, entitled "HIGH DENSITY SEMICONDUCTOR MEMORY CELL AND MEMORY ARRAY USING A SINGLE TRANSISTOR", to which priority from both is hereby claimed under 35 USC § 120.

now Patent No. 6,777,757

TECHNICAL FIELD OF THE INVENTION

[0002] The present invention relates to a nonvolatile programmable semiconductor memory, and more particularly to a single transistor memory cell programmed by break down of the transistor gate oxide, and a memory array incorporating such cells.

BACKGROUND OF THE INVENTION

[0003] Nonvolatile memory retains stored data when power is removed, which is desirable in many different types of electronic devices. One commonly available type of nonvolatile memory is the programmable read-only memory ("PROM"), which uses word line – bit line crosspoint elements such as fuses, anti-fuses, and trapped charge devices such as the floating gate avalanche injection metal oxide semiconductor ("FAMOS") transistor to store logical information.

[0004] An example of one type of PROM cell that uses the breakdown of a silicon dioxide layer in a capacitor to store digital data is disclosed in United States Patent No. 6,215,140 to Reisinger et al. The basic PROM disclosed by Reisinger et al. uses a series combination